IN THE CLAIMS

1. (currently amended): A non-optical electronic semiconductor device comprising:

a sapphire support substrate including at least one groove;

a first insulation layer on top of the support substrate;

an SOI layer formed on top of the first insulation layer; [[and]]

a first element layer formed on the SOI layer, [[;]]

wherein the at least one groove extends below a target element in the first element layer whose dielectric loss is to be controlled; ~~among the at least one element;~~

a second insulation layer formed on top of the first element layer; and

at least one additional element layer formed on top of the second insulation layer.

2. (currently amended): The semiconductor device according to claim 1, wherein the at least one groove is formed such that a ~~reverse~~ lower face of the first insulation layer is exposed.

3. (currently amended): The semiconductor device according to claim 1, wherein the ~~at least one~~ target element is an analog element.

4. (original): The semiconductor device according to claim 3, wherein the analog element is an inductor.

5. (canceled)

6. (currently amended): A non-optical electronic semiconductor device comprising:

a sapphire support substrate including at least one groove;

a first insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer; [[and]]

a plurality of analog elements formed on the SOI layer, [[;]]

wherein the at least one groove extends below one or more analog elements among the plurality of analog elements;

a second insulation layer formed over the plurality of analog elements; and

at least one additional element layer formed on top of the second insulation layer.

7. (currently amended): The semiconductor device according to claim 6, wherein the groove is formed such that a ~~reverse~~ lower face of the first insulation layer is exposed.

8. (previously presented): The semiconductor device according to claim 6, wherein the one or more analog elements are inductors.

9. (currently amended): The semiconductor device according to claim 6, wherein the ~~target element is an element~~ one or more analog elements are elements for which control of [[the]] dielectric loss is sought, among the plurality of analog elements.

10.-20. (canceled)

21. (new): A non-optical electronic semiconductor device comprising:

a support substrate including at least one groove;

a first insulation layer on top of the support substrate;

an SOI layer formed on top of the first insulation layer;

a first element layer formed in a first-element area on the SOI layer,

wherein the at least one groove extends below a target element in the first element layer whose dielectric loss is to be controlled;

a second insulation layer formed on top of the first element layer; and

at least one additional element layer formed on top of the second insulation layer;

the substrate further comprising a plurality of bonding pads surrounding the first-element area; and

wherein no groove is formed below the plurality of bonding pads.

22. (new): The semiconductor device according to claim 21, wherein the target element is a high-frequency circuit.

23. (new): The semiconductor device according to claim 21, wherein the support substrate is a sapphire substrate.

24. (new): The semiconductor device according to claim 21, wherein the at least one groove is formed such that a lower face of the first insulation layer is exposed.

25. (new): The semiconductor device according to claim 21, wherein the target element is an analog element.

26. (new): The semiconductor device according to claim 25, wherein the analog element is an inductor.

27. (new): A non-optical electronic semiconductor device comprising:

a support substrate including at least one groove;

a first insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer;

a plurality of analog elements formed in an analog-element area on the SOI layer,

wherein the at least one groove extends below one or more analog elements among the plurality of analog elements;

a second insulation layer formed over the plurality of analog elements; and

at least one additional element layer formed on top of the second insulation layer;

the substrate further comprising a plurality of bonding pads surrounding the analog-element area; and

wherein no groove is formed below the plurality of bonding pads.

28. (new): The semiconductor device according to claim 27, wherein said one or more analog elements are inductors.

29. (new): The semiconductor device according to claim 27, wherein said one or more analog elements are elements for which control of dielectric loss is sought.

30. (new): The semiconductor device according to claim 27, wherein the support substrate is a sapphire substrate.

31. (new): The semiconductor device according to claim 27, wherein the groove is formed such that a lower face of the first insulation layer is exposed.

32. (new): The semiconductor device according to claim 1, wherein the target element is a high-frequency circuit.